

DATA SHEET

TJA1054 Fault-tolerant CAN transceiver

Preliminary specification
File under Integrated Circuits, IC18

1999 Feb 11

Fault-tolerant CAN transceiver

TJA1054

FEATURES

Optimized for in-car low-speed communication

- Baud rate up to 125 kBaud
- Up to 32 nodes can be connected
- Supports unshielded bus wires
- Very low Radio Frequency Interference (RFI) due to built-in slope control function and a very good matching of the CANL and CANH bus outputs
- Fully integrated receiver filters
- Permanent dominant monitoring of transmit data input
- Good immunity performance of ElectroMagnetic Compatibility (EMC) in normal operating mode and in low power modes.

Bus failure management

- Supports single-wire transmission modes with ground offset voltages up to 1.5 V
- Automatic switching to single-wire mode in the event of bus failures, even when the CANH bus wire is short-circuited to V_{CC}
- Automatic reset to differential mode if bus failure is removed
- Fully wake-up capability during failure modes.

Protection

- Short-circuit proof to battery and ground in 12 V powered systems
- Thermally protected
- Bus lines protected against transients in an automotive environment
- An unpowered node does not disturb the bus lines.

Support for low power modes

- Low current sleep and standby mode with wake-up via the bus lines
- Power-on reset flag on the output.

GENERAL DESCRIPTION

The TJA1054 is the interface between the protocol controller and the physical wires of the bus lines in a Control Area Network (CAN). It is primarily intended for low-speed applications, up to 125 kBaud, in passenger cars. The device provides differential transmit capability but will switch in error conditions to single-wire transmitter and/or receiver.

The TJA1054T is pin and upwards compatible with the PCA82C252T and the TJA1053T. This means that these two devices can be replaced by the TJA1054T with retention of all functions.

The most important improvements are:

- Very low RFI due to a very good matching of the CANL and CANH bus lines outputs
- Good immunity performance of EMC, especially in low power modes
- Fully wake-up capability during failure modes
- Extended bus failure management including short-circuit of the CANH bus line to V_{CC}
- Supports easy fault localization
- Two-edge sensitive wake-up input signal via pin \overline{WAKE} .

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TJA1054T	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage on pin V_{CC}		4.75	–	5.25	V
V_{BAT}	battery voltage on pin BAT	no time limit	–0.3	–	+40	V
		operating mode	5.0	–	27	V
		load dump	–	–	40	V
I_{BAT}	battery current on pin BAT	Sleep mode; $V_{CC} = 0$ V; $V_{BAT} = 12$ V	–	30	50	μ A
V_{CANH}	CANH bus line voltage	$V_{CC} = 0$ to 5.5 V; $V_{BAT} \geq 0$ V; no time limit	–40	–	+40	V
V_{CANL}	CANL bus line voltage	$V_{CC} = 0$ to 5.5 V; $V_{BAT} \geq 0$ V; no time limit	–40	–	+40	V
ΔV_{CANH}	CANH bus line transmitter voltage drop	$I_{CANH} = -40$ mA	–	–	1.4	V
ΔV_{CANL}	CANH bus line transmitter voltage drop	$I_{CANL} = 40$ mA	–	–	1.4	V
t_{PD}	propagation delay	TXD to RXD	–	1	–	μ s
t_r	bus line output rise time	10 to 90%; $C_1 = 10$ nF	–	0.6	–	μ s
t_f	bus line output fall time	90 to 10%; $C_1 = 1$ nF	–	0.3	–	μ s
T_{amb}	operating ambient temperature		–40	–	+125	$^{\circ}$ C

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BLOCK DIAGRAM

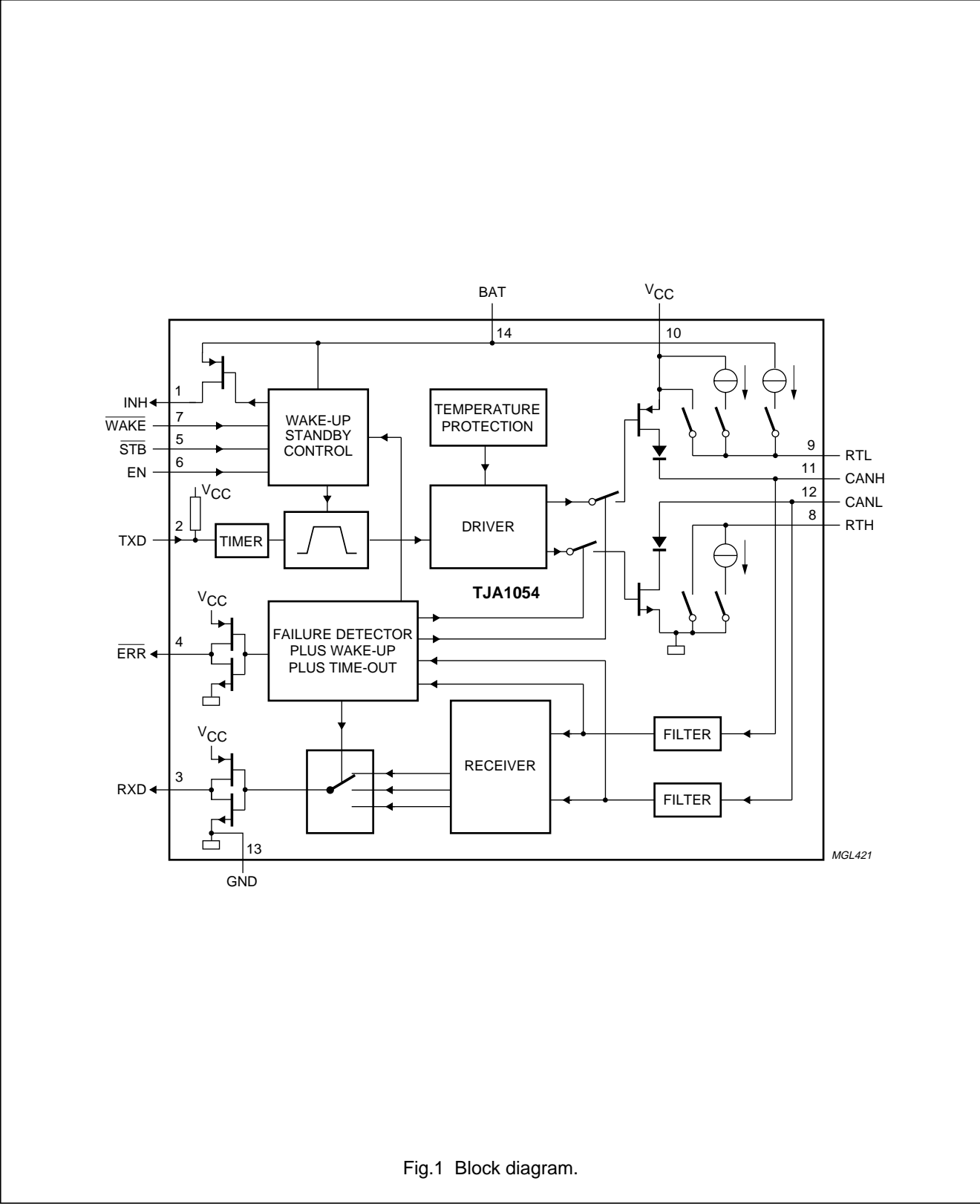


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
INH	1	inhibit output for switching an external voltage regulator if a wake-up signal occurs
TXD	2	transmit data input for activating the driver to the bus lines
RXD	3	receive data output for reading out the data from the bus lines
ERR	4	error, wake-up and power-on indication output; active LOW in normal operating mode when the bus has a failure and in low power modes (wake-up signal or in power-on standby)
STB	5	standby digital control signal input (active LOW); defines together with input signal on pin EN the state of the transceiver (in normal and low power modes); see Table 2 and Fig.3
EN	6	enable digital control signal input; defines together with input signal on pin STB the state of the transceiver (in normal and low power modes); see Table 2 and Fig.3
WAKE	7	local wake-up signal input; falling and rising edges are both detected
RTH	8	termination resistor connection; in case of a CANH bus wire error the line is terminated with a selectable impedance
RTL	9	termination resistor connection; in case of a CANL bus wire the line is terminated with a selectable impedance
V _{CC}	10	supply voltage
CANH	11	HIGH-level voltage bus line
CANL	12	LOW-level voltage bus line
GND	13	ground
BAT	14	battery supply

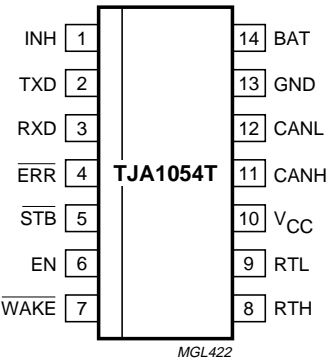


Fig.2 Pin configuration.

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FUNCTIONAL DESCRIPTION

The TJA1054 is the interface between the CAN protocol controller and the physical wires of the CAN bus (see Fig.7). It is primarily intended for low speed applications, up to 125 kBaud, in passenger cars. The device provides differential transmit capability to the CAN bus and differential receive capability to the CAN controller.

To reduce RFI, the rise and fall slope are limited. This allows the use of an unshielded twisted pair or a parallel pair of wires for the bus lines. Moreover, it supports transmission capability on either bus line if one of the wires is corrupted. The failure detection logic automatically selects a suitable transmission mode.

In normal operating mode (no wiring failures) the differential receiver is output on pin RXD (see Fig.1). The differential receiver inputs are connected to pins CANH and CANL through integrated filters. The filtered input signals are also used for the single-wire receivers. The receivers connected to pins CANH and CANL have threshold voltages that ensure a maximum noise margin in single-wire mode.

A timer has been integrated at pin TXD. This timer prevents the TJA1054 from driving the bus lines to a permanent dominant state.

Failure detector

The failure detector is fully active in the normal operating mode. After the detection of a single bus failure the detector switches to the appropriate mode (see Table 1).

Table 1 Bus failures

FAILURE	DESCRIPTION
1	CANH wire interrupted
2	CANL wire interrupted
3	CANH short-circuited to battery
3a	CANH short-circuited to V _{CC}
4	CANL short-circuited to ground
5	CANH short-circuited to ground
6	CANL short-circuited to battery
6a	CANL short-circuited to V _{CC}
7	CANL mutually short-circuited to CANH

The differential receiver threshold voltage is set at −3.2 V typically (V_{CC} = 5 V). This ensures correct reception with a noise margin as high as possible in the normal operating mode and in the event of failures 1, 2, 4 and 6a. These failures, or recovery from them, do not destroy ongoing transmissions.

Failures 3 and 6 are detected by comparators connected to the CANH and CANL bus lines, respectively. If the comparator threshold is exceeded for a certain period of time, the reception is switched to the single-wire mode. This time is needed to avoid false triggering by external RF fields. Recovery from these failures is detected automatically after a certain time-out (filtering) and no transmission is lost. In the event of failure 3 the CANH driver and pin RTH are switched off. In the event of failure 6 the CANL driver and pin RTL are switched off. The pull-up current on pin RTL and the pull-down current on pin RTH will not be switched off.

Failures 3a, 4 and 7 initially result in a permanent dominant level on pin RXD. After a time-out, the CANL driver and pin RTL are switched off (failures 4 and 7) or the CANH driver and pin RTH are switched off (failure 3a). Only a weak pull-up on pin RTL or a weak pull-down on pin RTH remains. Reception continues by switching to the single-wire mode via pins CANH or CANL. When failures 3a, 4 or 7 are removed, the recessive bus levels are restored. If the differential voltage remains below the recessive threshold level for a certain period of time, reception and transmission switch back to the differential mode.

If any of the wiring failure occurs, the output signal on pin $\overline{\text{ERR}}$ will become LOW. On error recovery, the output signal on pin $\overline{\text{ERR}}$ will become HIGH again.

During all single-wire transmissions, the EMC performance (both immunity and emission) is worse than in the differential mode. The integrated receiver filters suppress any HF noise induced into the bus wires. The cut-off frequency of these filters is a compromise between propagation delay and HF suppression. In the single-wire mode, LF noise cannot be distinguished from the required signal.

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Low power modes

The transceiver provides 3 low power modes which can be entered and exited via pins $\overline{\text{STB}}$ and EN (see Table 2 and Fig.3).

The Sleep mode is the mode with the lowest power consumption. Pin INH is switched to high-impedance for deactivation of the external voltage regulator. Pin CANL is biased to the battery voltage via pin RTL. If the supply voltage is provided pins RXD and $\overline{\text{ERR}}$ will signal the wake-up interrupt signal.

The standby mode will react the same as the Sleep mode but with a HIGH-level on pin INH.

The power-on standby mode is the same as the standby mode with the battery power-on flag instead of the wake-up interrupt signal on pin $\overline{\text{ERR}}$. The output on pin RXD will show the wake-up interrupt. This mode is only for reading out the power-on flag.

Wake-up requests are recognized by the transceiver when a dominant signal is detected on either bus line or if pin WAKE detects an edge (rising or falling) which stays longer HIGH or LOW respectively during a certain period of time. On a wake-up request the transceiver will set the output on pin INH which can be used to activate the external supply voltage regulator.

If V_{CC} is provided the wake-up request can be read on the $\overline{\text{ERR}}$ or RXD outputs, so the external microcontroller can wake-up the transceiver (switch to normal operating mode) via pins $\overline{\text{STB}}$ and EN.

To prevent false wake-up due to transients or RF fields, the wake-up voltage levels have to be maintained for a certain period of time. In the low power modes the failure detection circuit remains partly active to prevent an increased power consumption in the event of failures 3, 3a, 4 and 7.

Pin INH is set to floating only during the goto-sleep command and stays floating during the Sleep mode. If pin INH is set to floating, pin INH will not be set to HIGH-level again just by a mode change to normal operating mode. Pin INH will be set to HIGH-level by the following events only:

- power-on (V_{BAT} switching-on at cold start)
- rising or falling edge on pin $\overline{\text{WAKE}}$
- a message with 5 consecutive dominant bits during pin EN or pin $\overline{\text{STB}}$ is at LOW-level.

The signals on pins $\overline{\text{STB}}$ and EN will internally be set to LOW-level when V_{CC} is below a certain threshold voltage so providing fail safe functionality.

Table 2 Normal operating and low power modes

MODE	$\overline{\text{STB}}$	EN	$\overline{\text{ERR}}$		RXD		RTL SWITCHED TO
			LOW	HIGH	LOW	HIGH	
Goto-sleep command	0	1	wake-up interrupt signal; notes 2 and 3		wake-up interrupt signal; notes 2 and 3		V_{BAT}
Sleep	0	0 ⁽¹⁾					V_{BAT}
Standby	0	0					V_{BAT}
Power-on standby	1	0	V_{BAT} power-on flag; notes 2 and 4		wake-up interrupt signal; notes 2 and 3		V_{BAT}
Normal operating	1	1	error flag	no error flag	dominant received data	recessive received data	V_{CC}

Notes

1. In case the goto-sleep command was used before. When V_{CC} drops pin EN will become LOW, but this does not effect the internal functions due to the fail safe functionality.
2. If the supply voltage V_{CC} is present.
3. Wake-up interrupts are released when entering the normal operating mode.
4. V_{BAT} power-on flag will be reset when entering the normal operating mode.

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Power-on

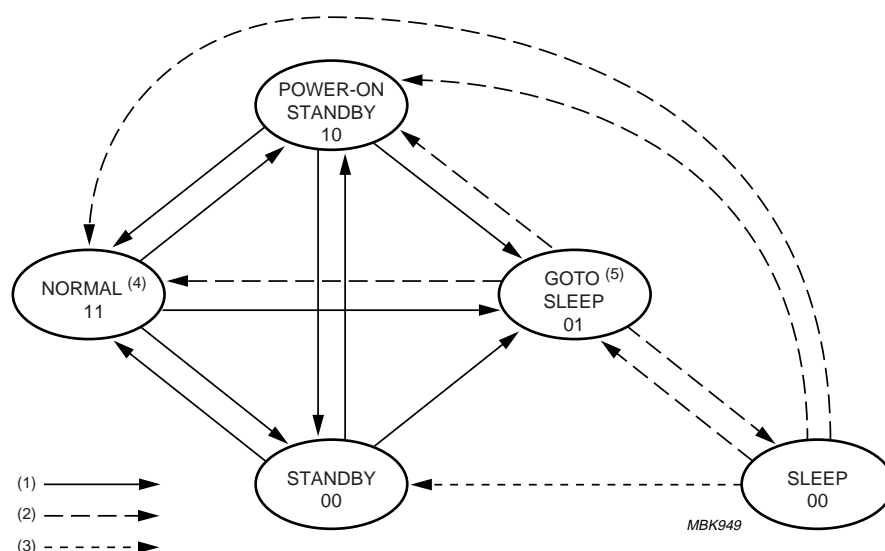
After power-on (V_{BAT} switched on) the signal on pin INH will become HIGH and an internal power-on flag will be set. This flag can be read in the power-on standby mode via pin \overline{ERR} ($\overline{STB} = 1$; $EN = 0$) and will be reset by entering the normal operating mode.

Protections

A current limiting circuit protects the transmitter output stages against short-circuit to positive and negative battery voltage.

If the junction temperature exceeds a maximum value, the transmitter output stages are disabled. Because the transmitter is responsible for the major part of the power dissipation, this will result in a reduced power dissipation and hence a lower chip temperature. All other parts of the IC will remain operating.

The pins CANH and CANL are protected against electrical transients which may occur in an automotive environment.



- (1) Mode change via input ports \overline{STB} and EN .
- (2) Mode change via input ports \overline{STB} and EN , but in the sleep mode INH is inactive and possibly there is no V_{CC} . Mode control is only possible if V_{CC} of the transceiver is active.
- (3) INH is activated after wake-up via bus or input port \overline{WAKE} .
- (4) Transitions to normal mode clear the internal wake-up: interrupt and battery fail flag are cleared.
- (5) Transitions to sleep mode: INH is deactivated.

Fig.3 Mode control.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CC}	supply voltage on pin V _{CC}		−0.3	+6	V
V _{BAT}	battery voltage on pin BAT		−0.3	+40	V
V _n	DC voltage on pins 2 to 6		−0.3	V _{CC} + 0.3	V
V _{CANH}	DC voltage on pin CANH		−40	+40	V
V _{CANL}	DC voltage on pin CANL		−40	+40	V
V _{trt(n)}	transient voltage on pins CANH and CANL	see Fig.6	−150	+100	V
V _{WAKE}	DC input voltage on pin $\overline{\text{WAKE}}$		−	V _{BAT} + 0.3	V
I _{WAKE}	DC input current on pin $\overline{\text{WAKE}}$		−15	−	mA
V _{INH}	DC output voltage on pin INH		−0.3	V _{BAT} + 0.3	V
V _{RTH}	DC voltage on pin RTH		−0.3	V _{BAT} + 1.2	V
V _{RTL}	DC voltage on pin RTL		−0.3	V _{BAT} + 1.2	V
R _{RTH}	termination resistance on pin RTH		500	16000	Ω
R _{RTL}	termination resistance on pin RTL		500	16000	Ω
T _{vj}	virtual junction temperature	note 2	−40	+150	°C
T _{stg}	storage temperature		−55	+150	°C
V _{esd}	electrostatic discharge voltage	human body model; note 3	−2.0	+2.0	kV
		machine model; note 4	−200	+200	V

Notes

1. All voltages are defined with respect to pin GND. Positive current flows into the IC.
2. Junction temperature in accordance with "IEC 747-1". An alternative definition is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$ where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of T_{vj} . The rating for T_{vj} limits the allowable combinations of power dissipation (P) and operating ambient temperature (T_{amb}).
3. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
4. Equivalent to discharging a 200 pF capacitor through a 10 Ω resistor and a 0.75 μH coil.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th(vj-a)}	thermal resistance from junction to ambient	in free air	120	K/W

QUALITY SPECIFICATION

Quality specification in accordance with "SNW-FQ-611-Part-E".

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DC CHARACTERISTICS

$V_{CC} = 4.75$ to 5.25 V; $V_{BAT} = 5$ to 27 V; $V_{STB} = V_{CC}$; $T_{amb} = -40$ to $+125$ °C; unless otherwise specified. All voltages are defined with respect to ground. Positive currents flow into the IC. All parameters are guaranteed over the temperature range by design, but only 100% tested at 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
I _{CC}	supply current	normal operating mode; V _{TXD} = V _{CC} (recessive)	4	7	11	mA
		normal operating mode; V _{TXD} = 0 V (dominant); no load	11	17	27	mA
		low power modes; V _{TXD} = V _{CC}	0	0	10	μA
I _{BAT}	battery current on pin BAT	all modes; in low power modes at V _{RTL} = V _{BAT} or V _{RTL} < 2.5 V (>1.5 ms) V _{BAT} = V _{WAKE} = V _{INH} = 12 V	10	30	50	μA
		V _{BAT} = V _{WAKE} = V _{INH} = 5 to 27 V	5	30	125	μA
		V _{BAT} = V _{WAKE} = V _{INH} = 3.5 V	5	20	30	μA
		V _{BAT} = V _{WAKE} = V _{INH} = 1 V	0	0	10	μA
I _{CC} + I _{BAT}	supply current plus battery current	low power modes; V _{CC} = 5 V; V _{BAT} = V _{WAKE} = V _{INH} = 12 V	–	35	60	μA
V _{BAT}	battery voltage on pin BAT	low power modes for setting power-on flag	–	–	1	V
		for not setting power-on flag	3.5	–	–	V
Pins STB, EN and TXD						
V _{IH}	HIGH-level input voltage		0.7V _{CC}	–	V _{CC} + 0.3	V
V _{IL}	LOW-level input voltage		–0.3	–	0.3V _{CC}	V
I _{IH}	HIGH-level input current pins $\overline{\text{STB}}$ and EN pin TXD	V _I = 4 V	–	9	20	μA
			–25	–80	–200	μA
I _{IL}	LOW-level input current pins $\overline{\text{STB}}$ and EN pin TXD	V _I = 1 V	4	8	–	μA
			–100	–320	–800	μA
V _{CC}	supply voltage	for forced power-on standby mode (fail safe)	2.75	–	4.5	V
Pins RXD and $\overline{\text{ERR}}$						
V _{OH}	HIGH-level output voltage on pin $\overline{\text{ERR}}$ on pin RXD	I _O = –100 μA	V _{CC} – 0.9	–	V _{CC}	V
		I _O = –1 mA	V _{CC} – 0.9	–	V _{CC}	V
V _{OL}	LOW-level output voltage on pins $\overline{\text{ERR}}$ and RXD	I _O = 1.6 mA	0	–	0.4	V
		I _O = 7.5 mA	0	–	1.5	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pin WAKE						
I_{IL}	LOW-level input current	$V_{WAKE} = 0\text{ V}$; $V_{BAT} = 27\text{ V}$	-1	-4	-10	μA
$V_{th(WAKE)}$	wake-up threshold voltage	$V_{STB} = 0\text{ V}$	2.5	3.2	3.9	V
Pin INH						
ΔV_H	HIGH-level voltage drop	$I_{INH} = -0.18\text{ mA}$	—	—	0.8	V
$ I_L $	leakage current	Sleep mode; $V_{INH} = 0\text{ V}$	—	—	5	μA
Pins CANH and CANL						
V_{diff}	differential receiver threshold voltage	no failures and bus failures 1, 2, 5, 6a; see Fig.4 $V_{CC} = 5\text{ V}$	-3.5	-3.2	-2.9	V
		$V_{CC} = 4.75\text{ to }5.25\text{ V}$	$-0.70V_{CC}$	$-0.64V_{CC}$	$-0.58V_{CC}$	V
$V_{O(reces)}$	recessive output voltage on pin CANH on pin CANL	$V_{TXD} = V_{CC}$ $R_{RTH} < 4\text{ k}\Omega$	—	—	0.2	V
		$R_{RTL} < 4\text{ k}\Omega$	$V_{CC} - 0.2$	—	—	V
$V_{O(dom)}$	dominant output voltage on pin CANH on pin CANL	$V_{TXD} = 0\text{ V}$; $V_{EN} = V_{CC}$ $I_{CANH} = -40\text{ mA}$	$V_{CC} - 1.4$	—	—	V
		$I_{CANL} = 40\text{ mA}$	—	—	1.4	V
$I_{O(CANH)}$	output current on pin CANH	normal operating mode; $V_{CANH} = 0\text{ V}$; $V_{TXD} = 0\text{ V}$	-45	-80	-110	mA
		low power modes; $V_{CANH} = 0\text{ V}$; $V_{CC} = 5\text{ V}$	—	-0.25	—	μA
$I_{O(CANL)}$	output current on pin CANL	normal operating mode; $V_{CANL} = 14\text{ V}$; $V_{TXD} = 0\text{ V}$	45	70	100	mA
		low power modes; $V_{CANL} = 12\text{ V}$; $V_{BAT} = 12\text{ V}$	—	0	—	μA
$V_{det(CANH)}$	detection threshold voltage for short-circuit to battery voltage on pin CANH	normal operating mode	1.5	1.7	1.85	V
		low power modes	1.1	1.8	2.5	V
$V_{det(CANL)}$	detection threshold voltage for short-circuit to battery voltage on pin CANL	normal operating mode	6.5	7.3	8	V
$V_{th(wake)}$	wake-up threshold voltage on pin CANL on pin CANH	low power modes	2.5	3.2	3.9	V
		low power modes	1.1	1.8	2.5	V
$\Delta V_{th(wake)}$	difference of wake-up threshold voltages	low power modes	0.8	1.4	—	V
$V_{se(CANH)}$	single-ended receiver threshold voltage on pin CANH	normal operating mode and failures 4, 6 and 7 $V_{CC} = 5\text{ V}$	1.5	1.7	1.85	V
		$V_{CC} = 4.75\text{ to }5.25\text{ V}$	$0.30V_{CC}$	$0.34V_{CC}$	$0.37V_{CC}$	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{se(CANL)}$	single-ended receiver threshold voltage on pin CANL	normal operating mode and failures 3 and 3a $V_{CC} = 5\text{ V}$ $V_{CC} = 4.75\text{ to }5.25\text{ V}$	3.15 $0.63V_{CC}$	3.3 $0.66V_{CC}$	3.45 $0.69V_{CC}$	V V
Pins RTH and RTL						
$R_{sw(RTL)}$	switch-on resistance between pin RTL and V_{CC}	normal operating mode; $ I_O < 10\text{ mA}$	–	50	100	Ω
$R_{sw(RTH)}$	switch-on resistance between pin RTH and ground	normal operating mode; $ I_O < 10\text{ mA}$	–	50	100	Ω
$V_{O(RTH)}$	output voltage on pin RTH	low power modes; $I_O = 1\text{ mA}$	–	0.7	1.0	V
$I_{O(RTL)}$	output current on pin RTL	low power modes; $V_{RTL} = 0\text{ V}$	–1.25	–0.65	–0.3	mA
$I_{pu(RTL)}$	pull-up current on pin RTL	normal operating mode and failures 4, 6 and 7	–	75	–	μA
$I_{pd(RTH)}$	pull-down current on pin RTH	normal operating mode and failures 3 and 3a	–	75	–	μA
Thermal shutdown						
T_j	junction temperature	for shutdown	155	165	180	$^{\circ}\text{C}$

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TIMING CHARACTERISTICS

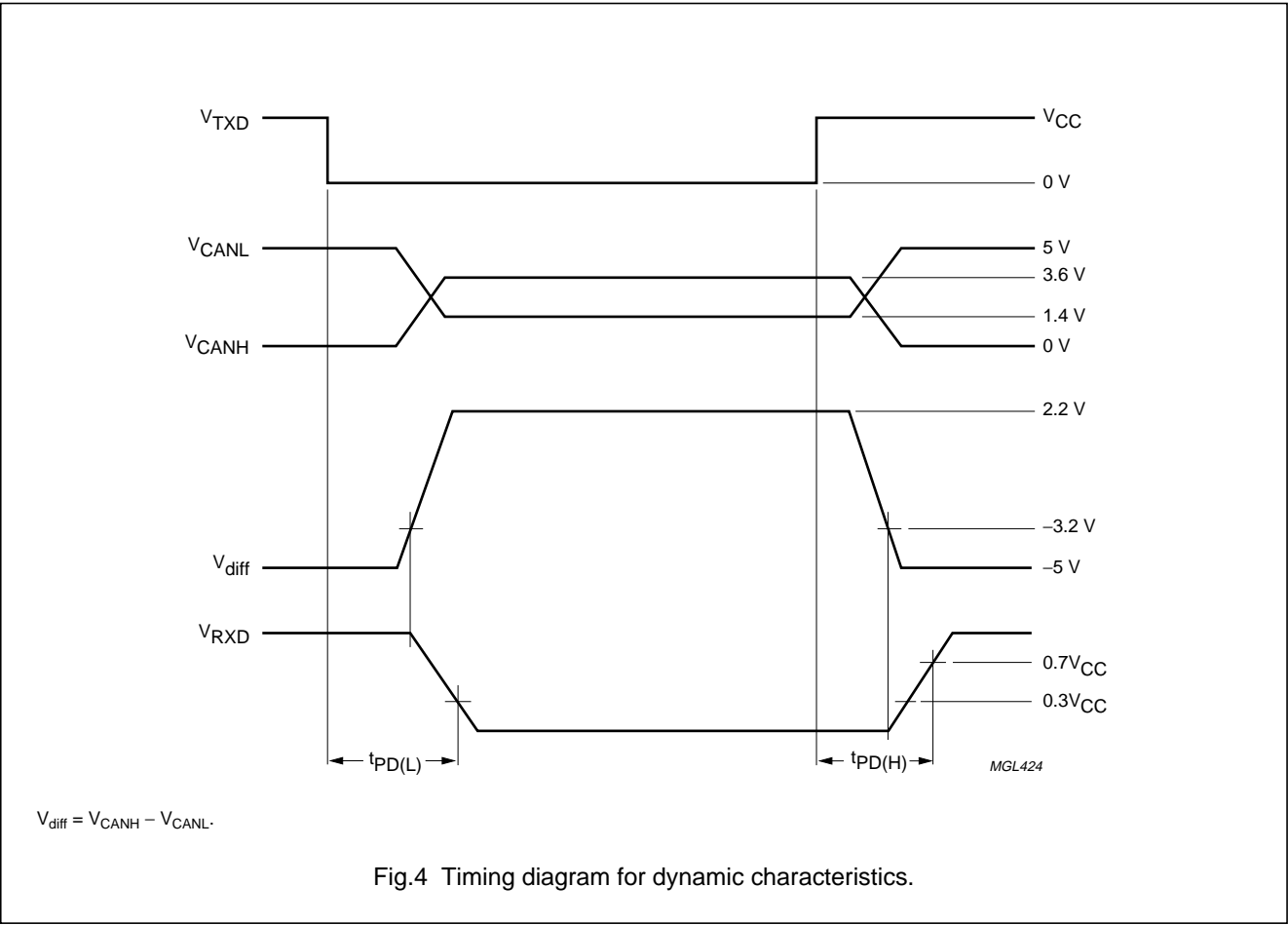
$V_{CC} = 4.75$ to 5.25 V; $V_{BAT} = 5$ to 27 V; $V_{STB} = V_{CC}$; $T_{amb} = -40$ to $+125$ °C; unless otherwise specified. All voltages are defined with respect to ground. Positive currents flow into the IC. All parameters are guaranteed over the temperature range by design, but only 100% tested at 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{t(r-d)}$	CANL and CANH output transition time for recessive-to-dominant	10 to 90%; C1 = 10 nF; C2 = 0; R1 = 100 Ω ; see Fig.5	0.35	0.60	—	μ s
$t_{t(d-r)}$	CANL and CANH output transition time for dominant-to-recessive	10 to 90%; C1 = 1 nF; C2 = 0; R1 = 100 Ω ; see Fig.5	0.2	0.3	—	μ s
$t_{PD(L)}$	propagation delay TXD to RXD (LOW)	no failures and failures 1, 2, 5, 6a; see Figs 4 and 5				
		C1 = 1 nF; C2 = 0; R1 = 100 Ω	—	0.75	1.35	μ s
		C1 = C2 = 3.3 nF; R1 = 100 Ω	—	1	1.75	μ s
		failures 3, 3a, 4, 6 and 7; see Figs 4 and 5				
$t_{PD(H)}$	propagation delay TXD to RXD (HIGH)	no failures and failures 1, 2, 5, 6a; see Figs 4 and 5				
		C1 = 1 nF; C2 = 0; R1 = 100 Ω	—	1.2	1.9	μ s
		C1 = C2 = 3.3 nF; R1 = 100 Ω	—	2.5	3.3	μ s
		failures 3, 3a, 4, 6 and 7; see Figs 4 and 5				
$t_{CANH(min)}$	minimum dominant time for wake-up on pin CANH	low power modes; $V_{BAT} = 12$ V	7	—	38	μ s
$t_{CANL(min)}$	minimum dominant time for wake-up on pin CANL	low power modes; $V_{BAT} = 12$ V	7	—	38	μ s
$t_{WAKE(min)}$	minimum time on pin \overline{WAKE}	low power modes; $V_{BAT} = 12$ V; for wake-up after receiving a falling or rising edge	7	—	38	μ s
t_{det}	failure detection time	normal mode				
		failure 3 and 3a	1.6	—	8.0	ms
		failure 4, 6 and 7	0.3	—	1.6	ms
		low power modes; $V_{BAT} = 12$ V				
		failure 3 and 3a	1.6	—	8.0	ms
		failure 4 and 7	0.1	—	1.6	ms

Fault-tolerant CAN transceiver

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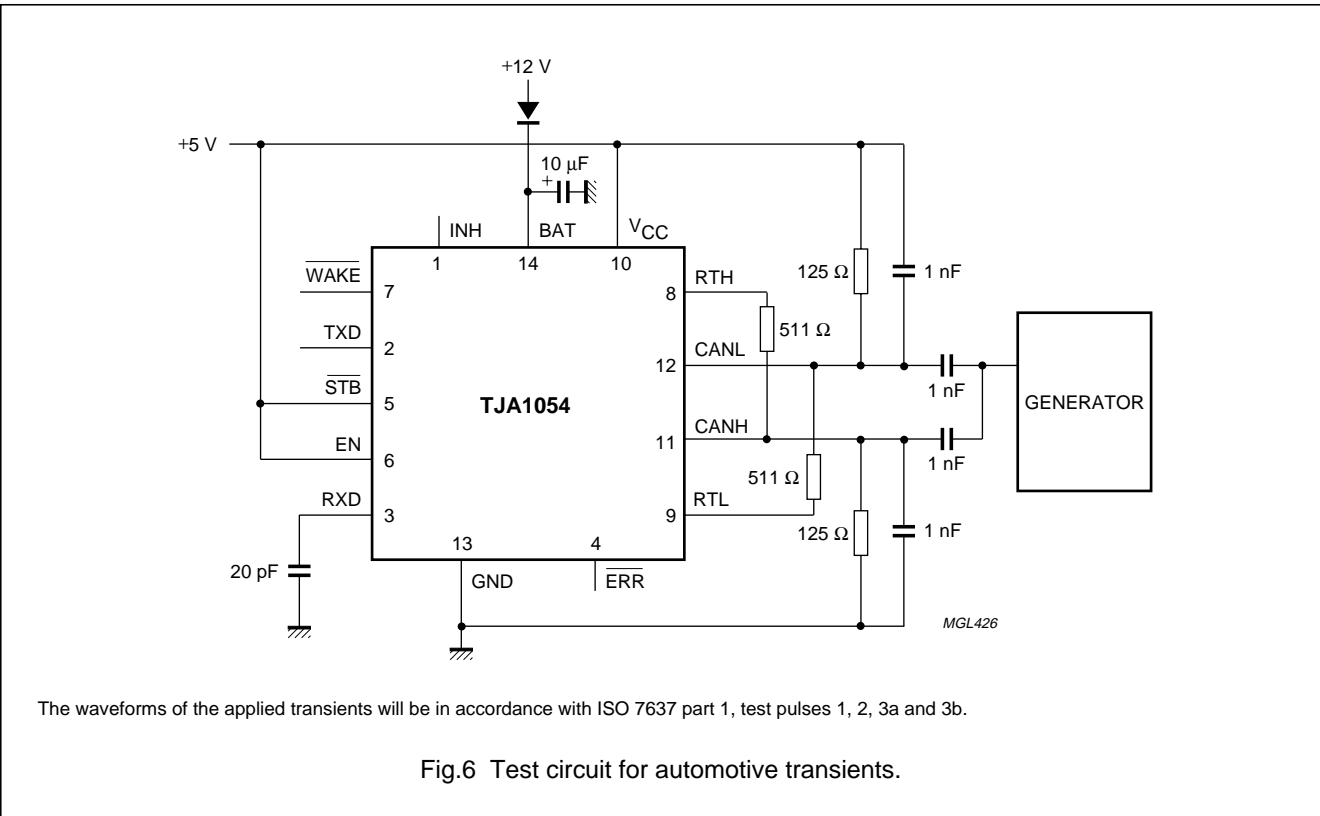
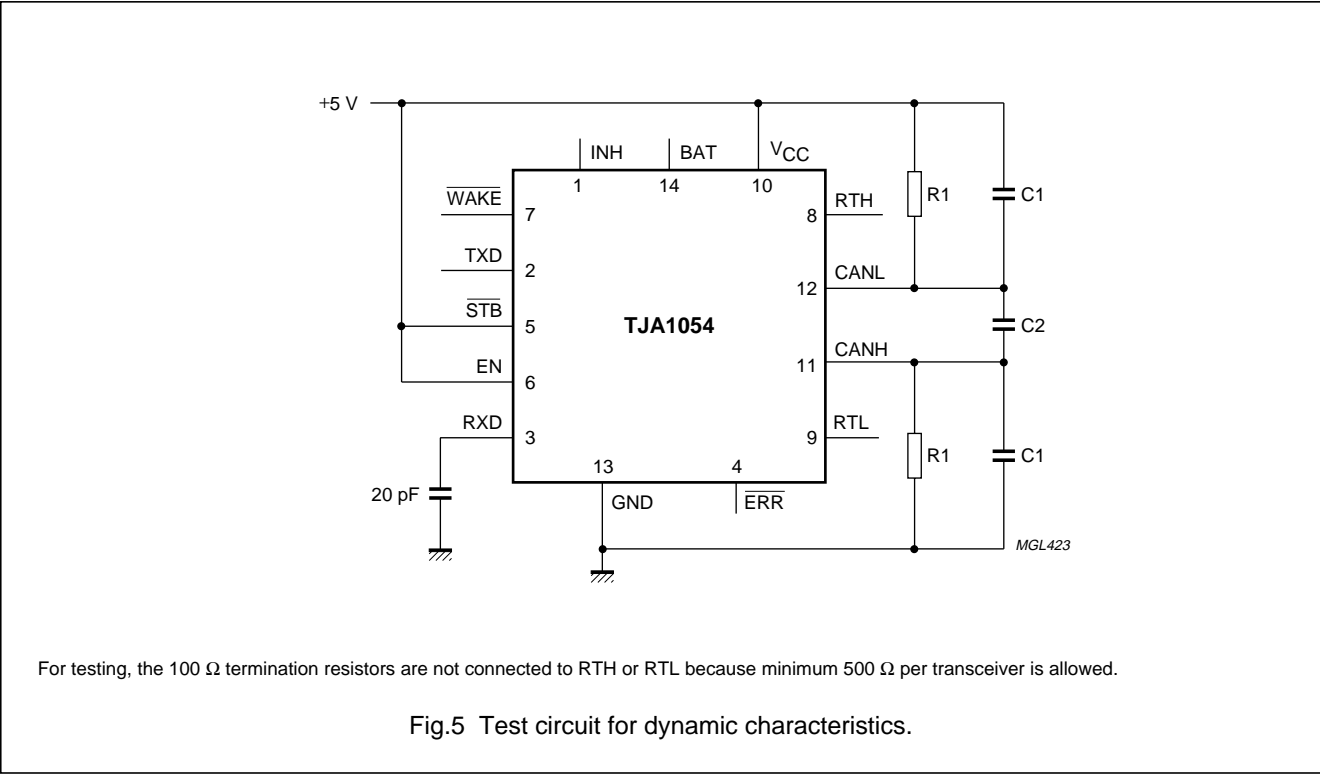
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{rec}	failure recovery time	normal mode				
		failure 3 and 3a	0.3	–	1.6	ms
		failure 4 and 7	7	–	38	μs
		failure 6	125	–	750	μs
		low power modes; $V_{\text{BAT}} = 12\text{ V}$				
		failures 3, 3a, 4 and 7	0.3	–	1.6	ms
$t_{\text{h(min)}}$	minimum hold time of goto-sleep command		5	–	50	μs
$t_{\text{dis(TXD)}}$	disable time of TXD permanent dominant timer	normal mode; $V_{\text{TXD}} = 0\text{ V}$	0.75	–	4	ms
Δpc	pulse-count difference between CANH and CANL	normal mode and failures 1, 2, 5 and 6a				
		failure detection (pin ERR becomes LOW)	–	4	–	
		failure recovery	–	4	–	



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TEST AND APPLICATION INFORMATION



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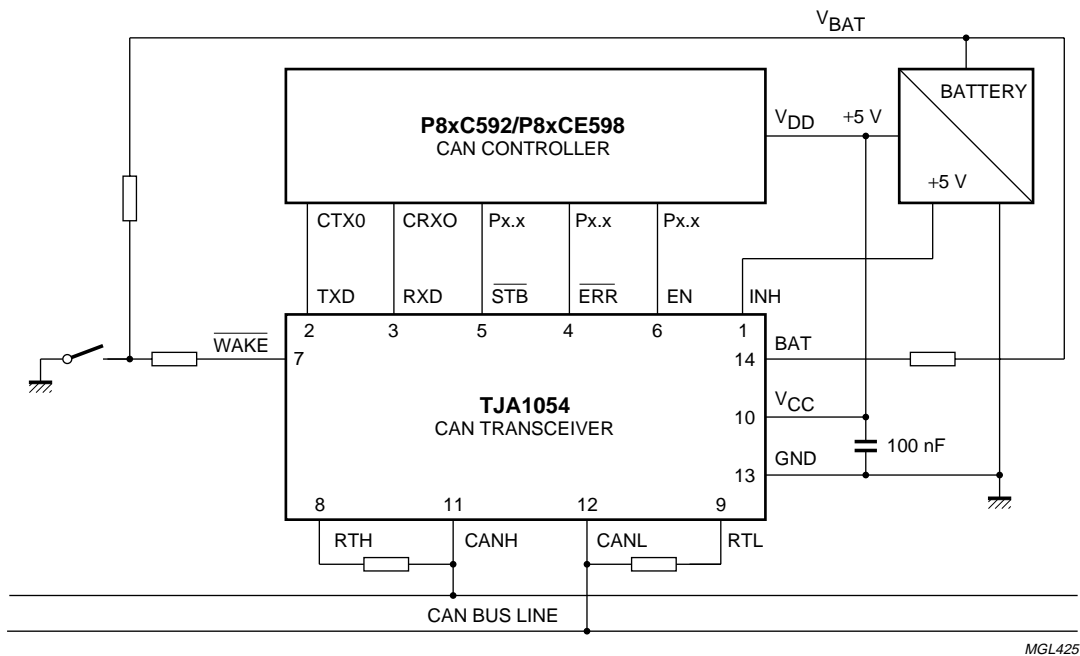


Fig.7 Application diagram.

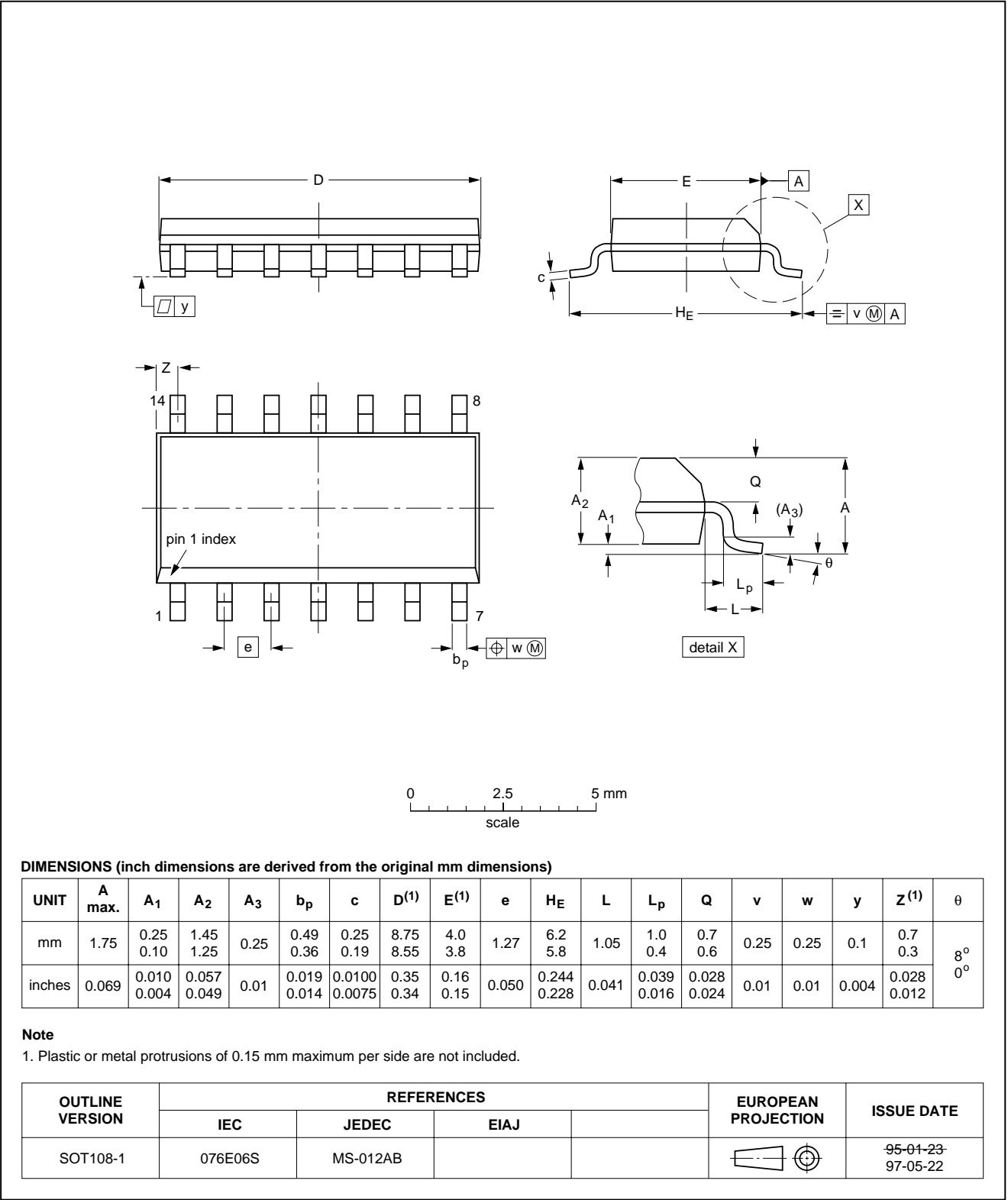
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PACKAGE OUTLINE

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



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SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW ⁽¹⁾
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable ⁽²⁾	suitable
PLCC ⁽³⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽³⁾⁽⁴⁾	suitable
SSOP, TSSOP, VSO	not recommended ⁽⁵⁾	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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